



Docket No.: 32481P001C

UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

MUKESH K. PATEL, ET AL.

Application No.: 09/938,886

Filed: August 24, 2001

For: **Java Virtual Machine Hardware For RISC
and CISC Processors**

Art Group: Unassigned

Examiner: Unassigned

#13/EP5
4-29-04

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INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted before the mailing of a first Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Copies of the references cited on PTO/SB/08 are enclosed herewith.

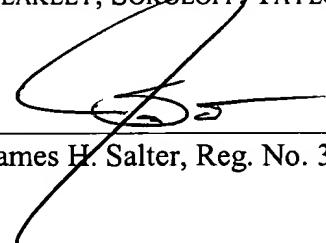
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

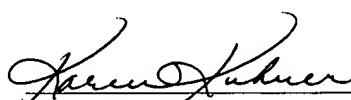
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 10/3/03


James H. Salter, Reg. No. 35,668

12400 Wilshire Blvd., 7th Floor
Los Angeles, California 90025
(408) 720-8300

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Karen Kuhner

10-03-03

Date



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet

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2

<i>Complete if Known</i>	
Application Number	09/938,886
Filing Date	August 24, 2001
First Named Inventor	Mukesh K. Patel
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	32481P001C

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

Examiner Signature		Date Considered	
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¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Sheet

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of

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Complete if Known

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Application Number	09/938,886
Filing Date	August 24, 2001
First Named Inventor	Mukesh K. Patel
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	32481P001C

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		R.M. TOMASULO, An Efficient Algorithm For Exploiting Multiple Arithmetic Units, IBM Journal of Research and Development, Vol. 11, No. 1, January 1967, pp. 25-27.	
		C. JOHN GLOSSNER and Stamatios Vassiliadis, The DELFT-JAVA Engine: An Introduction, Euro-Par' 97 Parallel Processing, Third International Euro-Par Conference Passau, Germany, August 26-29, 1997 Proceedings, pp. 767-770.	
		M. WATHEQ EL-KHARASHI and FAYEZ ELGUIBALY, Java Microprocessors: Computer Architecture Implications, 1997 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, PACRIM, Victoria, BC, Canada, August 20-22, 1997, pp. 277-280.	
		A.C. ROSE, Hardware JAVA Accelerator, for the ARM7, Fourth year Undergraduate project in Group d, 1996/1997, pp. 1-48 plus Appendix.	
		OTTO STEINBUSCH, Designing Hardware to Interpret Virtual Machine Instructions, Department of Electrical Engineering of Eindhoven University of Technology, Philips Semiconductors 1998, Master's Degree Thesis, February 1998.	

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